Nuvoton

NCT5945Y

NCT5945W

4-channel I^{2}C-bus switch with interrupt logic and reset

Revision: 1.0 Date: July, 2017

NCT5945Y/W Datasheet Revision History

	PAGES	DATES	VERSION	WEB VERSION	MAIN CONTENTS
1	N.A.	6th, Oct.	0.5		Preliminary Version
2	6	4th, May	0.6		Update the description of control register
3	20-21	6th, June	0.7		Update the ordering information and add the taping spec
4	19-20	6th, Oct.	0.8		Update1MHz (Fast-mode plus) spec.
5		14th, July	1.0		Update to public verison

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1. GENERAL DESCRIPTION

The NCT5945Y/W is a quad bidirectional translating switch which can be controlled via the I^2C-bus. The SCL/SDA upstream pair fans out to eight downstream pairs, or channels. Any individual SCx/SDx channel or combination of channels can be selected, determined by the contents of the programmable control register. Four interrupt inputs, INT0_N to INT3_N, one for each of the downstream pairs, are provided. One interrupt output, INT_N, acts as an AND of the four interrupt inputs.

The system master can reset the NCT5945Y/W in the event of a timeout or other improper operation by asserting a low in the RESET_N input. Equally, the power-on reset deselects all channels and initializes the I^2C state machine. Asserting RESET_N causes the same reset or initialization to occur without powering down the part.

The pass gates of the switches are constructed such that the VDD pin can be used to limit the maximum high voltage which be passed by the NCT5945Y/W. This allows the use of different bus voltages on each pair, so that 1.8V or 2.5V or 3.3V parts can communicate with 5V parts without any additional protection. External pull-up resistors pull the bus up to the desired voltage level for each channel. All I/O are 5V tolerant.

2. FEATURES

2.1 General Features

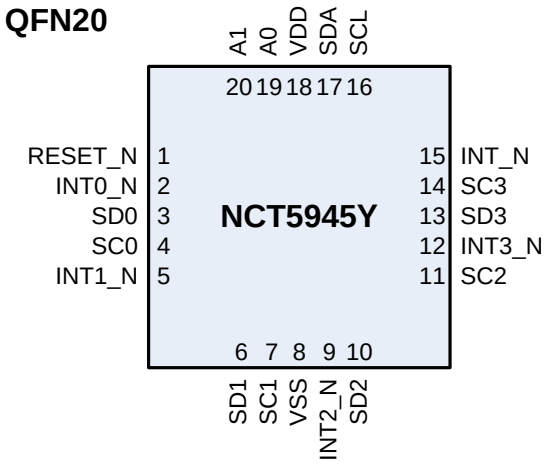
- 1-of-4 bidirectional translating switches
- I^2C-bus interface logic; compatible with SMBus standards
- Four active low interrupt inputs
- Active low interrupt output
- Active low reset input
- Two dedicated hardware address pins for use of up to four devices
- Channel selection via I^2C-bus, in any combination
- Power-up with all switch channels deselected
- Low R_{on} switches
- Allows voltage level translation between 1.8V, 2.5V, 3.3V and 5V buses
- No glitch on power-up
- Supports hot insertion
- Low standby current
- Operating power supply voltage range of 2.3V to 5.5V
- 5V tolerant inputs
- 0 Hz to 1MHz clock frequency
- ESD protection exceeds 2000V HBM per JESD22-A114 and 1000V CDM per JESD22-C101
- Latch-up protection exceeds 100mA per JESD78
- Two packages offered: QFN20 and TSSOP20

2.2 Key Specifications

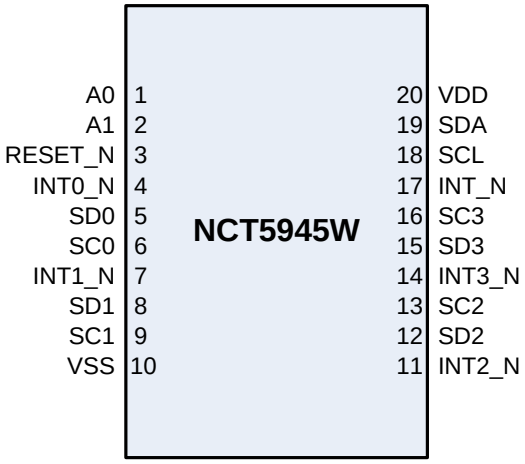
- Supply Voltage is 2.3 V to 5.5 V
- Standby Current is 1uA max.
- Operating Temperature is from -40 ˚C to 85 ˚C

3. PIN CONFIGURATION

QFN20



TSSOP20



4. PIN DESCRIPTION

Symbol	Pin		Description
	TSSOP20	QFN20	
A0	1	19	Address input 0. Connect directly to VDD or VSS.
A1	2	20	Address input 1. Connect directly to VDD or VSS.
RESET_N	3	1	Active LOW reset input. Connect to VDD through a pull-up resistor, if not used.
INT0_N	4	2	Active low interrupt input 0
SD0	5	3	Serial data 0. Connect to VDD through a pull-up resistor.
SC0	6	4	Serial clock 0. Connect to VDD through a pull-up resistor.
INT1_N	7	5	Active low interrupt input 1
SD1	8	6	Serial data 1. Connect to VDD through a pull-up resistor.
SC1	9	7	Serial clock 1. Connect to VDD through a pull-up resistor.
VSS	10	8	Supply ground
INT2_N	11	9	Active low interrupt input 2
SD2	12	10	Serial data 2. Connect to VDD through a pull-up resistor.
SC2	13	11	Serial clock 2. Connect to VDD through a pull-up resistor.
INT3_N	14	12	Active low interrupt input 3
SD3	15	13	Serial data 3. Connect to VDD through a pull-up resistor.
SC3	16	14	Serial clock 3. Connect to VDD through a pull-up resistor.
INT_N	17	15	Active low interrupt output. Connect to VDD through a pull-up resistor.
SCL	18	16	Serial clock line. Connect to VDD through a pull-up resistor.
SDA	19	17	Serial data line. Connect to VDD through a pull-up resistor.
VDD	20	18	Supply voltage

5. BLOCK DIAGRAM

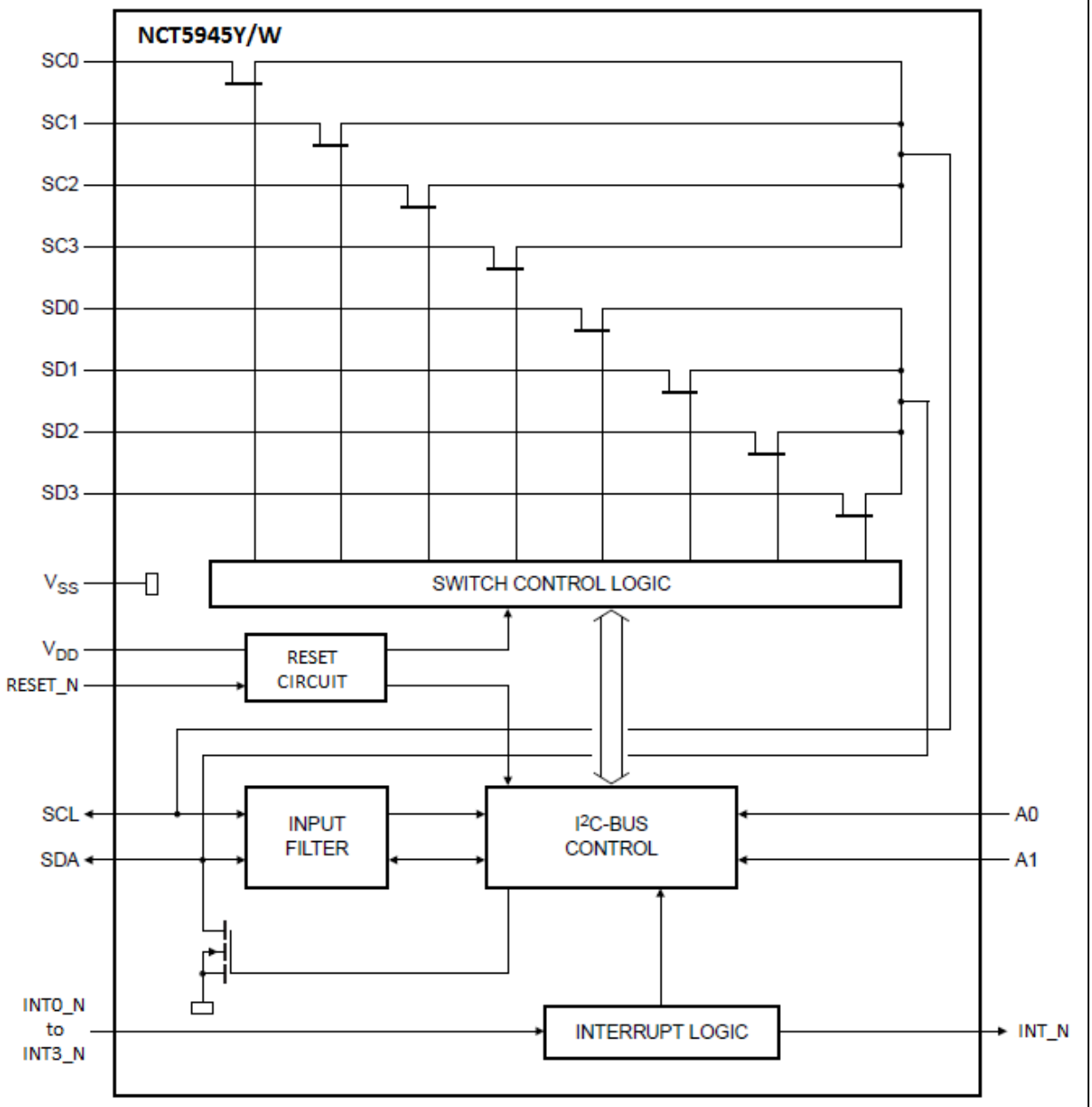


Figure 5. Block diagram of NCT5945Y/W

6. FUNCTION DESCRIPTIONS

6.1 Device address

Following a start condition, the bus master must output the address of the slave which it is accessing. The address of the NCT5945Y/W is shown in Figure 6-1. To conserve power, no internal pull-up resisters are incorporated on the hardware selectable address pins and they must be pulled high or low.

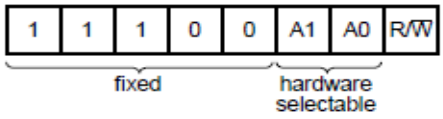


Figure 6-1. Slave address

The last bit of the slave address defines the operation (read or write) to be performed. When it is logic high, a read is selected, while logic low selects a write operation.

Address reference table:

Inputs		I^2C bus slave address (1,1,1,0,0,A1,A0)
A1	**A0**	
L	L	70h
L	H	71h
H	L	72h
H	H	73h

6.2 Control register

Following the successful acknowledgement of the slave address byte, the bus master will send a command byte which is stored in the control register in the NCT5945Y/W (see Figure 6-2). This register can be written and read via the I^2C-bus. Each bit in the command byte corresponds to a SCn/SDn channel and a high selects this channel. Multiple SCn/SDn channels may be selected at the same time. When a channel is selected, the channel becomes active after a stop condition has been placed on the I^2C-bus. This register can be written and read via the I^2C-bus.

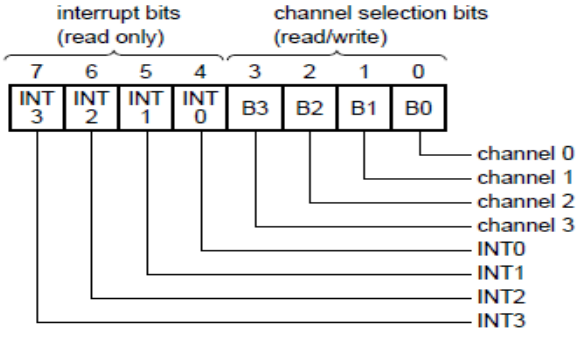


Figure 6-2. Control register

6.2.1 Control register definition

This register can be written and read via the I^2C-bus. Each bit in the command byte corresponds to a SCx/SDx channel and a high selects this channel. Multiple SCx/SDx channels may be selected at the same time. When a channel is selected, the channel becomes active after a stop condition has been placed on the I^2C-bus. This ensures that all SCx/SDx lines are in a high state when the channel is made active, so that no false conditions are generated at the time of connection. A stop condition always must occur immediately after the acknowledge cycle.

Table 6-1. Control register: write (channel selection); read (channel status)

INT3	INT2	INT1	INT0	B3	B2	B1	B0	Command
X	X	X	X	X	X	X	0	channel 0 disabled
							1	channel 0 enabled
X	X	X	X	X	X	0	X	channel 1 disabled
						1		channel 1 enabled
X	X	X	X	X	0	X	X	channel 2 disabled
					1			channel 2 enabled
X	X	X	X	0	X	X	X	channel 3 disabled
				1				channel 3 enabled
0	0	0	0	0	0	0	0	No channel selected, power-up/reset default state

Remark: Multiple channels can be enabled at the same time. Example: B3 = 0, B2 = 1, B1 = 1, B0 = 0, means that channels 3 and 0 are disabled, and channels 2 and 1 are enabled. Care should be taken not to exceed the maximum bus capacity.

6.3 Interrupt handling

The NCT5945Y/W provides 4 interrupt inputs, one for each channel, and one open-drain interrupt output. When an interrupt is generating by any device, it will be detected by the NCT5945Y/W and the interrupt output will be driven low. The channel does not need to be active for detection of the interrupt. A bit is also set in the control register.

Bit 4 through bit 7 of the control register corresponds to channel 0 through channel 3 of the NCT5945Y/W, respectively. Therefore, if an interrupt is generated by any device connected to channel 1, the state of the interrupt inputs is loaded into the control register when a read is accomplished. Likewise, an interrupt on any device connected to channel 0 would cause bit 4 of the control register to be set on the read. The master can then address the NCT5945Y/W and read the contents of the control register to determine which channel contains the device generating the interrupt. The master can then reconfigure the NCT5945Y/W to select this channel, and locate the device generating the interrupt and clear it.

It should be noted that more than one device can provide an interrupt on a channel, so it is up to the master to ensure that all devices on a channel are interrogated for an interrupt.

The interrupt inputs may be used as general-purpose inputs if the interrupt function is not required.

If unused, interrupt input(s) must be connected to V_{DD} through a pull-up resistor.

Table 6-2. Control register: read (interrupt)

INT3	INT2	INT1	INT0	B3	B2	B1	B0	Command
X	X	X	0	X	X	X	X	No interrupt on channel 0
			1					Interrupt on channel 0
X	X	0	X	X	X	X	X	No interrupt on channel 1
		1						Interrupt on channel 1
X	0	X	X	X	X	X	X	No interrupt on channel 2
	1							Interrupt on channel 2
0	X	X	X	X	X	X	X	No interrupt on channel 3
1								Interrupt on channel 3

Remark: Several channels can be active at the same time. Example: INT3_N = 0, INT2_N = 1, INT1_N = 1, INT0_N = 0, means that there is no interrupt on channel 0 and channel 3, and there is interrupt on channel 1 and channel 2.

6.4 RESET_N input

The RESET_N input is an active low signal that may be used to recover from a bus fault condition. When this signal is asserted low for a minimum of $t_{w(rst)L}$, the NCT5945Y/W will reset its registers and I^2C-bus state machine and will deselect all channels. The RESET_N input must be connected to VDD through a pull-up resistor.

6.5 Power-on reset

When power (from 0V) is applied to VDD, an internal power-on reset holds the NCT5945Y/W in a reset condition until VDD has reached V_{POR}. At that point, the reset condition is released and the NCT5945Y/W registers and I^2C-bus state machine are initialized to their default states (all zeros) causing all the channels to be deselected. After that, VDD must be lowered to below 0.2V and then back up to the operating voltage for a power reset cycle.

6.6 Voltage translation

The pass gate transistors of the NCT5945Y/W are constructed such that the VDD voltage can be used to limit the maximum voltage that will be passed from one I^2C-bus to another. Figure 6-5 shows the voltage characteristics of the pass gate transistors (note that the graph was generated using the data specified in Section 9 “DC Characteristics” of this data sheet).

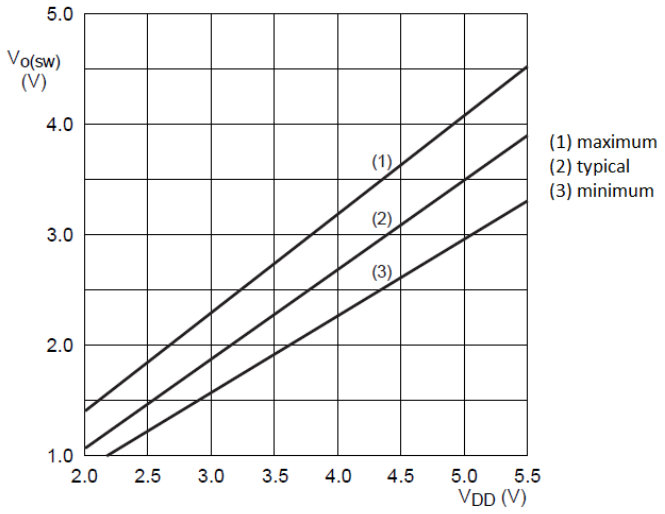


Figure 6-5. Pass gate voltage versus supply voltage

For the NCT5945Y/W to act as a voltage translator, the $V_{o(sw)}$ voltage should be equal to, or lower than the lowest bus voltage. For example, if the main bus was running at 5 V, and the downstream buses were 3.3 V and 2.7 V, then $V_{o(sw)}$ should be equal to or below 2.7 V to effectively clamp the downstream bus voltages. As shown in Figure 6-5, $V_{o(sw)(max)}$ will be 2.7 V when the NCT5945Y/W supply voltage is 3.5 V or lower, so the NCT5945Y/W supply voltage could be set to 3.3 V. Pull-up resistors can then be used to bring the bus voltages to their appropriate levels (see Figure 8).

7. CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resister when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

7.1 Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high period of the clock pulse as changes in the data line at this time will be interrupted as control signals (see Figure 7-1).

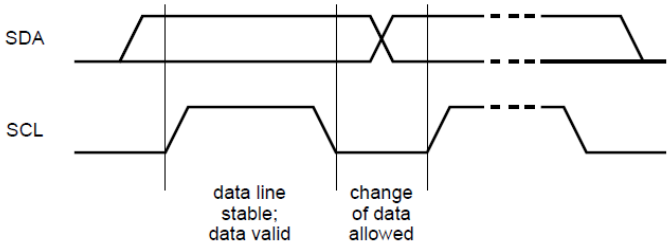


Figure 7-1. Bit transfer

7.2 START and STOP Conditions

Both data and clock lines remain high when the bus is not busy. A high-to-low transition of the data line, while the clock is high is defined as the START condition (S). A low-to-high transition of the data line while the clock is high is defined as the STOP condition (P) (see Figure 7-2).

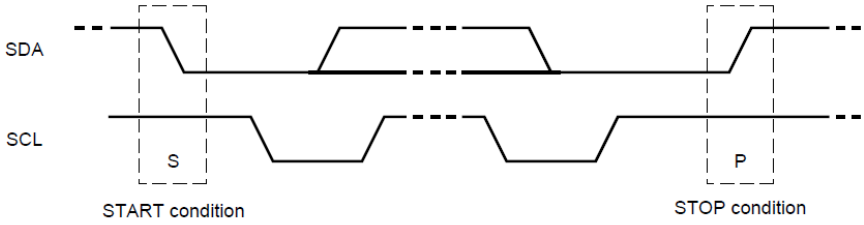


Figure 7-2. Definition of START and STOP conditions

7.3 System Configuration

A device generating a message is a “transmitter”, and a device receiving is the “receiver”. The device which controls the message is the “master” and the devices which are controlled by the master are the “slaves” (see Figure 7-3).

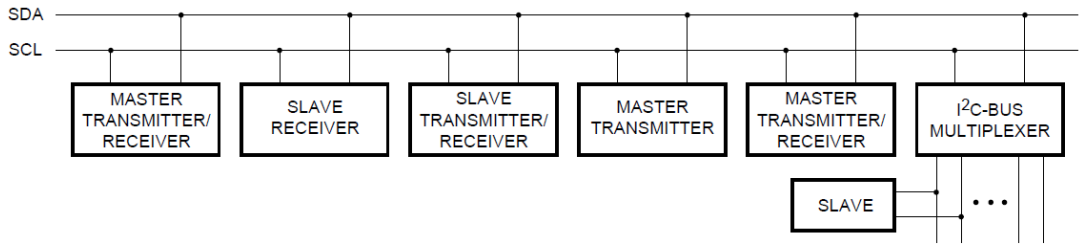


Figure 7-3. System configuration

7.4 Acknowledge

The number of data bytes transferred between the START and the STOP conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a high level put on the bus by the transmitter, whereas the master generates an extra acknowledge related clock pulse.

A slave receiver addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device which acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable low during the high period of the acknowledge related clock pulse. Set-up and hold times must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte which has been clocked out of the slave. In this event, the transmitter must leave the data line high to enable the master to generate a STOP condition.

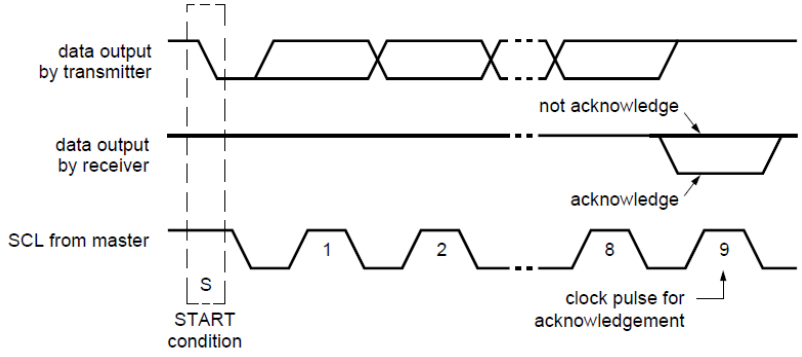


Figure 7-4. Acknowledgement on the bus

7.5 Bus Transactions

Data is transmitted to the NCT5945Y/W by sending the device address and setting the LSB to a logic 0 (see Figure 6-1). The command byte is sent after the address and determines which SCx/SDx channel receives the data which follows the command byte (see Figure 7-5). There is no limitation on the number of data bytes sent in one write transmission.

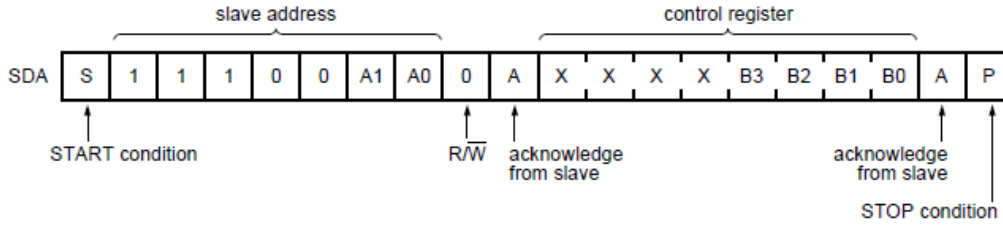


Figure 7-5. Write control register

The bus master first must send the NCT5945Y/W address with the LSB set to a logic 1 (see Figure 6-1). The command byte is sent after the address and determines which SCx/SDx channel is accessed. After a restart, the device address is sent again, but this time, the LSB is set to a logic 1. Data from the SCx/SDx channel defined by the command byte then is sent by the NCT5945Y/W (see Figure 7-6). After a restart, the value of the SCx/SDx channel defined by the command byte matches the SCx/SDx channel being accessed when the restart occurred. Data is clocked into the SCx/SDx channel on the rising edge of the acknowledge clock pulse. There is no limitation on the number of data bytes received in one read transmission, but when the final byte is received, the bus master must not acknowledge the data.

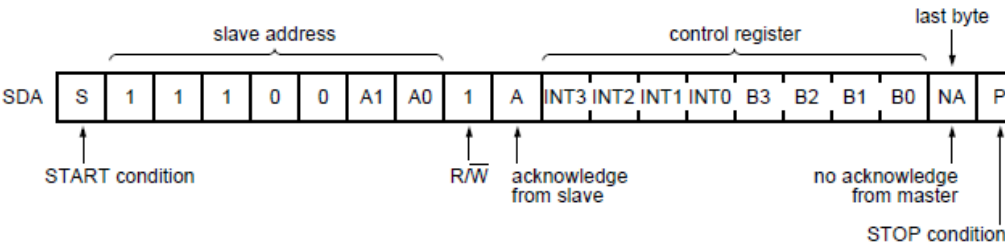


Figure 7-6. Read control register

8. APPLICATION

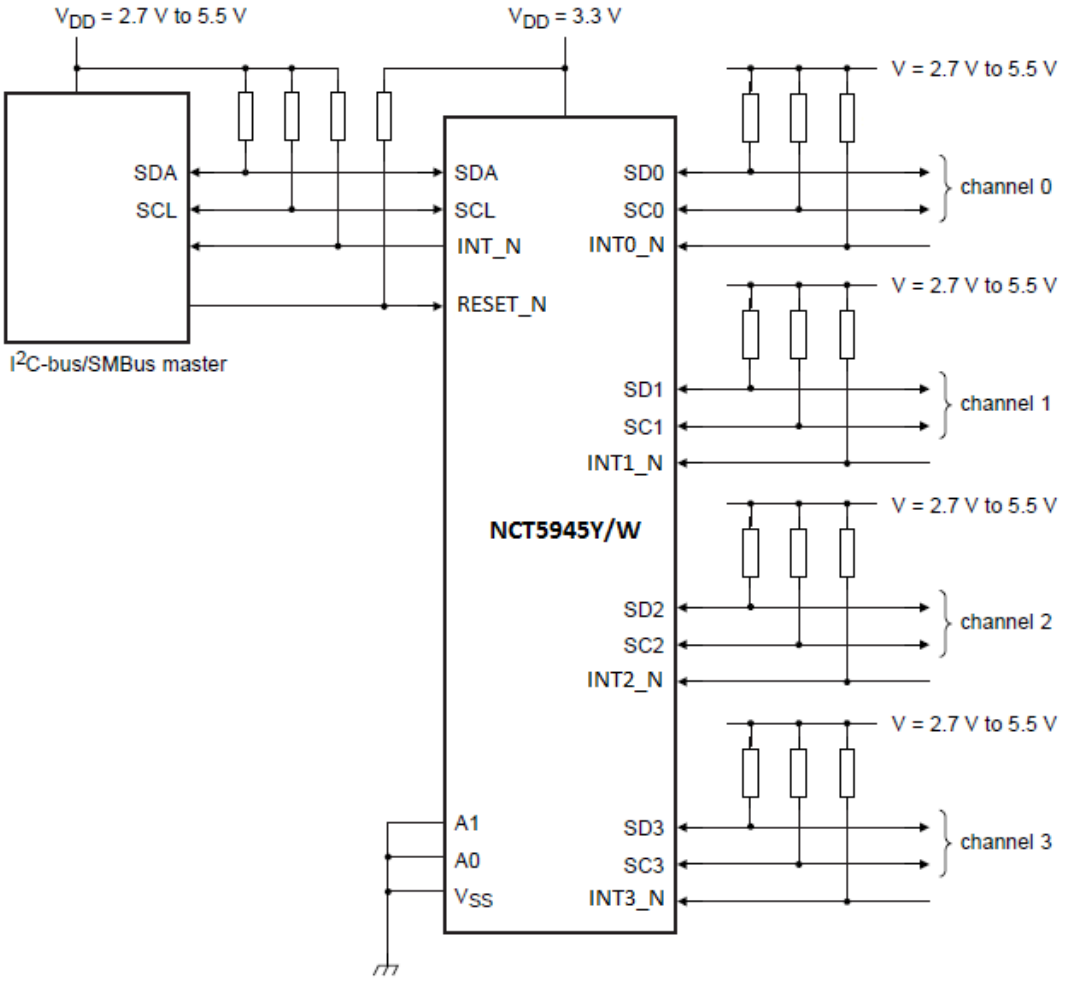


Figure 8. Typical application

9. DC AND AC SPECIFICATION

9.1 Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Power Supply Voltage	2.3 to 5.5	V
Input Voltage	2.3 to 5.5	V
Operating Temperature *1	-40 to +85	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

Note *1: Guaranteed by design from -40~85 degreeC, 100% tested at 85 degreeC.

9.2 DC Characteristics

9.2.1 T_{amb} = -40°C to 85°C, VDD = 2.3V to 3.6V, VSS = 0V

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Supply						
V_{DD}	Supply Voltage		2.3	-	3.6	V
I_{DD}	Supply Current	Operating mode; V_{DD}=3.6V; no load; V_I=V_{DD} or V_{SS}; f_{SCL}=100KHz	-	10	30	uA
I_{stb}	Standby Current	Standby mode; V_{DD}=3.6V; no load; V_I=V_{DD} or V_{SS}	-	0.1	1	uA
V_{POR}	Power-on Reset Voltage	no load; V_I=V_{DD} or V_{SS}	-	1.6	2.1	V
Input SCL; Input/Output SDA						
V_{IL}	Low-level Input Voltage		-0.5	-	+0.3V_{DD}	V
V_{IH}	High-level Input Voltage		0.7V_{DD}	-	6	V
I_{OL}	Low-level Output Current	V_{OL}=0.4V V_{OL}=0.6V	3 6	7 10	- -	mA mA
I_L	Leakage Current	V_I=V_{DD} or V_{SS}	-1	-	+1	uA
C_i	Input Capacitance	V_I=V_{SS}	-	10	13	pF
Select Inputs A0 to A1; INT0_N to INT3_N; RESET_N						
V_{IL}	Low-level Input Voltage		-0.5	-	+0.3V_{DD}	V

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{IH}	High-level Input Voltage		$0.7V_{DD}$	-	6	V
I_{LI}	Input Leakage Current	pin at V_{DD} or V_{SS}	-1	-	+1	uA
C_i	Input Capacitance	$V_I=V_{SS}$	-	1.6	3	pF
Pass Gate						
R_{on}	On-State Resistance	V_{DD}=3.0V to 3.6V; V_O=0.4V; I_O=15mA V_{DD}=2.3V to 2.7V; V_O=0.4V; I_O=10mA	5 7	11 16	30 55	Ω Ω
$V_{o(sw)}$	Switch Output Voltage	$V_{i(sw)}=V_{DD}$=3.3V;$I_{o(sw)}$= -100uA	-	1.9	-	VV
		$V_{i(sw)}=V_{DD}$=3.0V to 3.6V; $I_{o(sw)}$= -100uA	1.6	-	2.8	V
		$V_{i(sw)}=V_{DD}$=2.5V; $I_{o(sw)}$= -100uA	-	1.5	-	V
		$V_{i(sw)}=V_{DD}$=2.3V to 2.7V; $I_{o(sw)}$=-100uA	1.1	-	2.0	V
I_L	Leakage Current	$V_I=V_{DD}$ or V_{SS}	-1	-	+1	uA
C_{io}	Input/Output Capacitance	$V_I=V_{SS}$	-	3	5	pF
INT_N output						
I_{OL}	Low-level output current	V_{OL}=0.4V	3	-	-	mA
I_{OH}	High-level output current		-	-	+10	uA

9.2.2 T_{amb} = -40°C to 85°C, VDD = 4.5V to 5.5V, VSS = 0V

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Supply						
V_{DD}	Supply Voltage		4.5	-	5.5	V
I_{DD}	Supply Current	Operating mode; V_{DD}=5.5V; no load; V_I=V_{DD} or V_{SS}; f_{SCL}=100KHz	-	25	100	uA
I_{stb}	Standby Current	Standby mode; V_{DD}=5.5V; no load; V_I=V_{DD} or V_{SS}	-	0.3	1	uA
V_{POR}	Power-on Reset Voltage	no load; V_I=V_{DD} or V_{SS}	-	1.7	2.1	V
Input SCL; Input/Output SDA						
V_{IL}	Low-level Input Voltage		-0.5	-	+0.3V_{DD}	V
V_{IH}	High-level Input Voltage		0.7V_{DD}	-	6	V
I_{OL}	Low-level Output Current	V_{OL}=0.4V V_{OL}=0.6V	3 6	- -	- -	mA mA
I_L	Leakage Current	V_I=V_{DD} or V_{SS}	-1	-	+1	uA
C_i	Input Capacitance	V_I=V_{SS}	-	10	13	pF
Select Inputs A0 to A1; INT0_N to INT3_N; RESET_N						
V_{IL}	Low-level Input Voltage		-0.5	-	+0.3V_{DD}	V
V_{IH}	High-level Input Voltage		0.7V_{DD}	-	6	V
I_{LI}	Input Leakage Current	pin at V_{DD} or V_{SS}	-1	-	+1	uA
C_i	Input Capacitance	V_I=V_{SS}	-	2	5	pF
Pass Gate						
R_{on}	On-state Resistance	V_{DD}=4.5V to 5.5V; V_O=0.4V; I_O=15mA	4	9	24	Ω
$V_{o(sw)}$	Switch Output Voltage	$V_{i(sw)}$=V_{DD}=5.0V; $I_{o(sw)}$= -100uA	-	3.6	-	V
		$V_{i(sw)}$=V_{DD}=4.5V to 5.5V; $I_{o(sw)}$= -100uA	2.6	-	4.5	V
I_L	Leakage Current	V_I=V_{DD} or V_{SS}	-1	-	+1	uA
C_{io}	Input/Output Capacitance	V_I=V_{SS}	-	3	5	pF
INT_N output						
I_{OL}	Low-level output current	V_{OL}=0.4V	3	-	-	mA
I_{OH}	High-level output current		-	-	+10	uA

9.3 AC Characteristics

Symbol	Parameter	Conditions	Standard-mode		Fast-mode		Unit
			Min.	Max.	Min.	Max.	
t_{PD}	Propagation Delay	From SDA to SDx, or SCL to SCx	-	0.3	-	0.3	ns
f_{SCL}	SCL Clock Frequency		0	100	0	400	kHz
t_{BUF}	Bus free time between a STOP and START condition		4.7	-	1.3	-	us
$t_{HD;STA}$	Hold time (repeated) START condition		4.0	-	0.6	-	us
t_{LOW}	Low Period of the SCL Clock		4.7	-	1.3	-	us
t_{HIGH}	High Period of the SCL Clock		4.0	-	0.6	-	us
$t_{SU;STA}$	Set-up Time for a repeated START condition		4.7	-	0.6	-	us
$t_{SU;STO}$	Set-up Time for STOP condition		4.0	-	0.6	-	us
$t_{HD;DAT}$	Data Hold Time		0	3.45	0	0.9	us
$t_{SU;DAT}$	Data Set-up Time		250	-	100	-	ns
t_r	Rise Time of both SDA and SCL Signals		-	1000	$20+0.1C_b$	300	ns
t_f	Fall Time of both SDA and SCL Signals		-	300	$20+0.1C_b$	300	ns
C_b	Capacitive Load for each bus line		-	400	-	400	pF
t_{SP}	Pulse Width of spikes that must be suppressed by the input filter		-	50	-	50	ns
$t_{VD;DAT}$	Data Valid Time	HIGH-to-LOW LOW-to-HIGH	- -	1 0.6	- -	1 0.6	us us
$t_{VD;ACK}$	Data Valid Acknowledge Time		-	1	-	1	us
INT_N							
$t_{v(INTn\_N-INT\_N)}$	Valid time from INTn_N to INT_N signal		-	4	-	4	us

Symbol	Parameter	Conditions	Standard-mode		Fast-mode		Unit
			Min.	Max.	Min.	Max.	
$t_{d(INTn\_N-INT\_N)}$	Delay time from INTn_N to INT_N inactive		-	2	-	2	us
RESET_N							
$t_{w(rst)L}$	Low-level Reset Time		4	-	4	-	ns
t_{rst}	Reset Time	SDA clear	500	-	500	-	ns
$t_{REC;STA}$	Recovery Time to START Condition		0	-	0	-	ns

Symbol	Parameter	Conditions	Fast-mode plus		Unit
			Min.	Max.	
t_{PD}	Propagation Delay	From SDA to SDx, or SCL to SCx	-	0.3	ns
f_{SCL}	SCL Clock Frequency		0	1000	kHz
t_{BUF}	Bus free time between a STOP and START condition		0.5	-	us
$t_{HD;STA}$	Hold time (repeated) START condition		0.26	-	us
t_{LOW}	Low Period of the SCL Clock		0.5	-	us
t_{HIGH}	High Period of the SCL Clock		0.26	-	us
$t_{SU;STA}$	Set-up Time for a repeated START condition		0.26	-	us
$t_{SU;STO}$	Set-up Time for STOP condition		0.26	-	us
$t_{HD;DAT}$	Data Hold Time		0	-	us
$t_{SU;DAT}$	Data Set-up Time		50		ns
t_r	Rise Time of both SDA and SCL Signals		-	120	ns
t_f	Fall Time of both SDA and SCL Signals		20+0.1C_b	120	ns
C_b	Capacitive Load for each bus line			550	pF
t_{SP}	Pulse Width of spikes that must be suppressed by the input filter		0	50	ns
$t_{VD;DAT}$	Data Valid Time	HIGH-to-LOW LOW-to-HIGH	-	0.45	us us
$t_{VD;ACK}$	Data Valid Acknowledge Time		-	0.45	us
INT_N					
$t_{v(INTn\_N-INT\_N)}$	Valid time from INTn_N to INT_N signal		-	4	us
$t_{d(INTn\_N-INT\_N)}$	Delay time from INTn_N to INT_N inactive		-	2	us
RESET_N					
$t_{w(rst)L}$	Low-level Reset Time		100	-	ns
t_{rst}	Reset Time	SDA clear	500	-	ns
$t_{REC;STA}$	Recovery Time to START Condition		0	-	ns

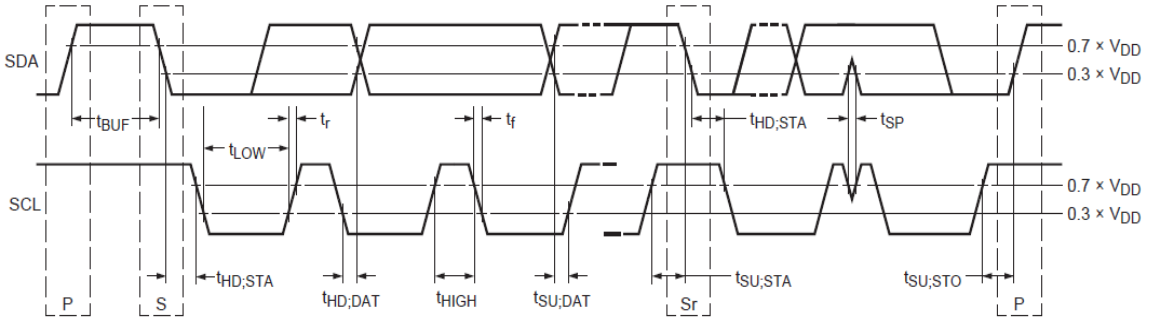


Figure 9-1. Definition of timing on the bus

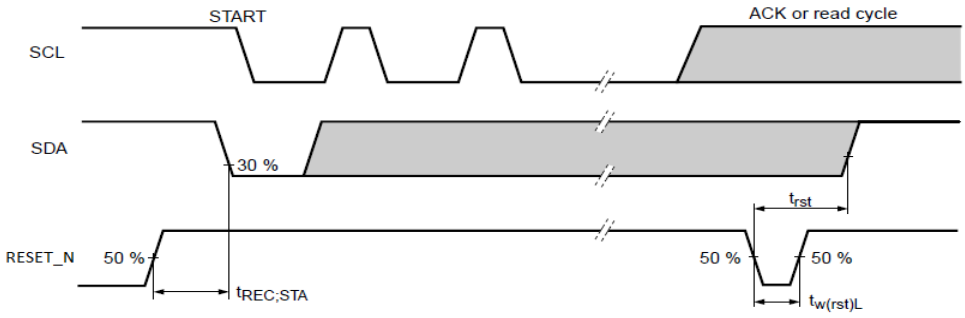


Figure 9-2. Definition of RESET_N timing

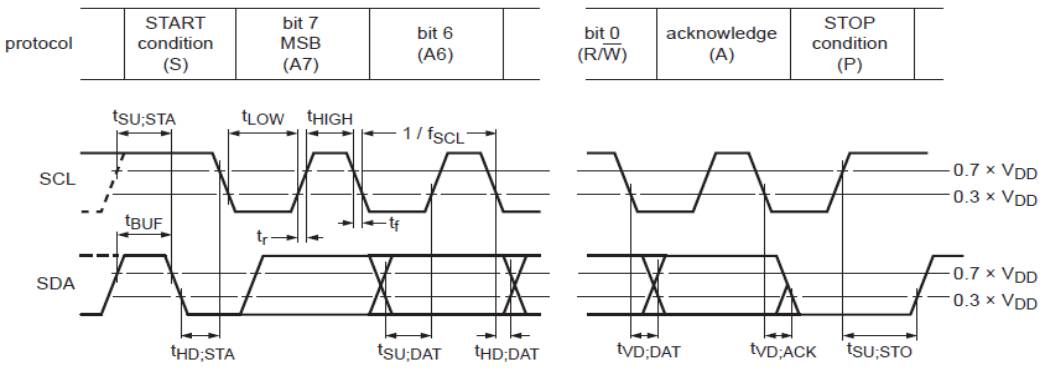


Figure 9-3. Bus timing diagram

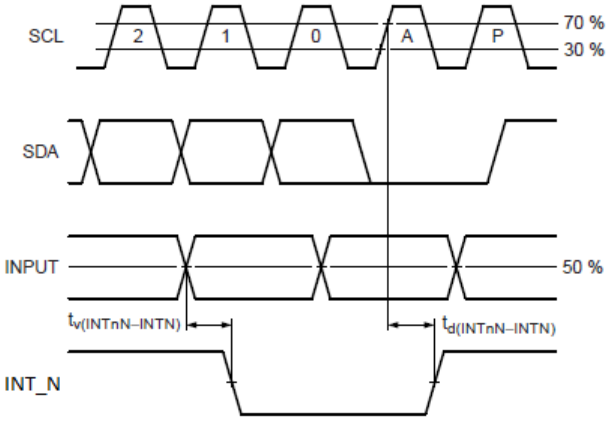


Figure 9-4. Read input port register

10. ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	SUPPLIED AS	PRODUCTION FLOW
NCT5945Y	QFN20	E Shape (Tray) T Shape (T&R), MOQ=4Kpcs	Commercial Grade
NCT5945W	TSSOP20	E Shape (Tube) T Shape (T&R), MOQ=2.5Kpcs	Commercial Grade

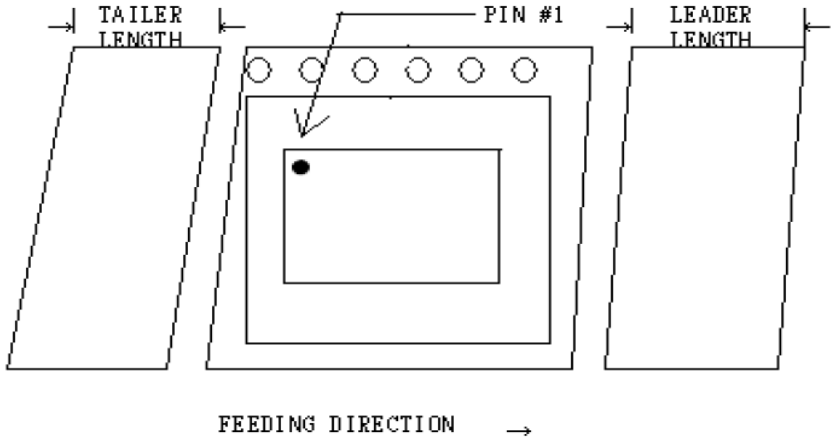
11. TOP MARKING SPECIFICATION

1st line: Nuvoton logo
2nd line: Part number: **NCT5945Y**
3rd line: Assembly tracking code
530: Package made in year 2015, week 30
G: Assembly house code
A: IC Version
SB: Nuvoton Internal use code

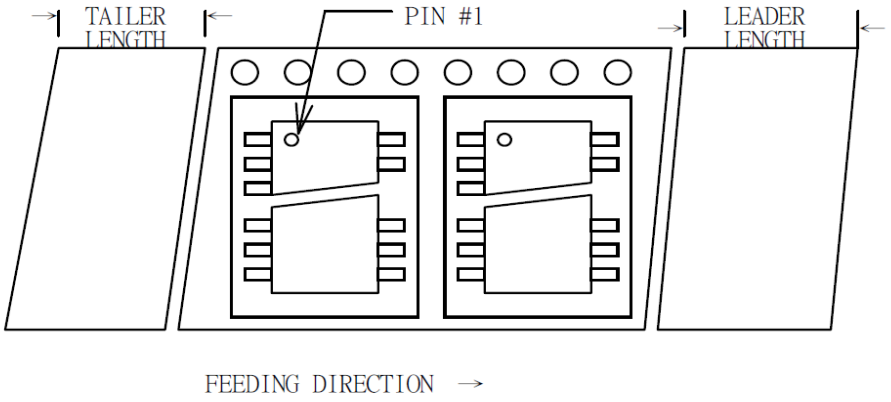
1st line: Nuvoton logo
2nd line: Part number: **NCT5945W**
3rd line: Assembly tracking code
530: Package made in year 2015, week 30
G: Assembly house code
A: IC Version
SB: Nuvoton Internal use code

12. TAPING SPECIFICATION

12.1 QFN 20L 5X5 mm^2



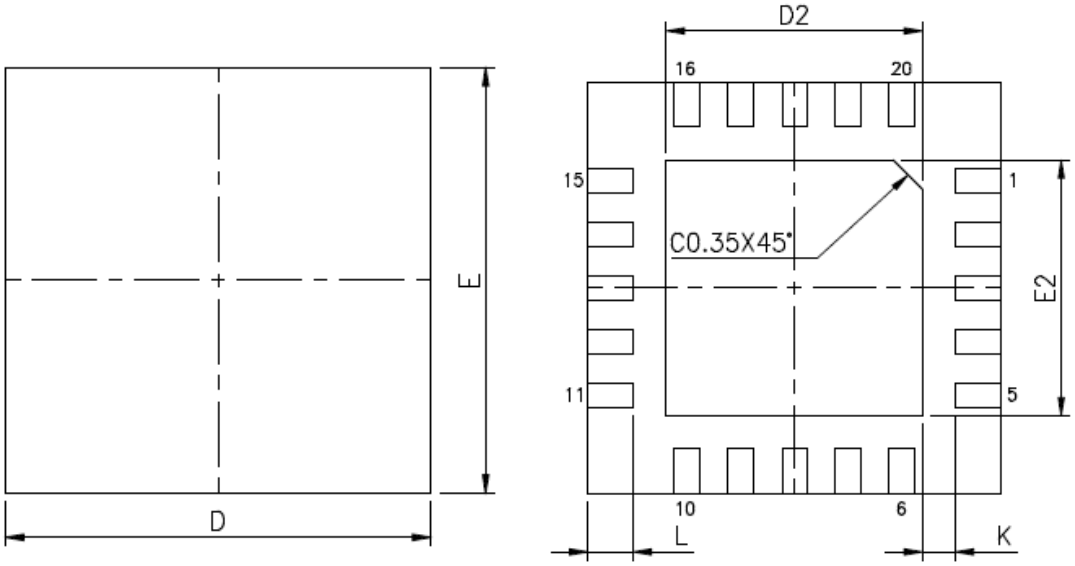
12.2 TSSOP 20L 4.4x6.5 MM^2

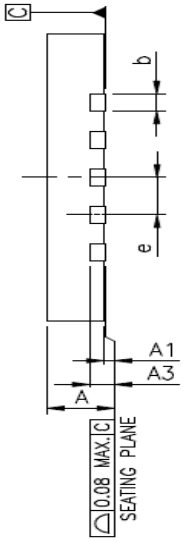


13. PACKAGE DIMENSION OUTLINE

13.1 QFN 20L 5X5 mm^2

Thickness: 0.8 mm (Max), Pitch: 0.65 mm, EP Size 3.1x3.1mm^2

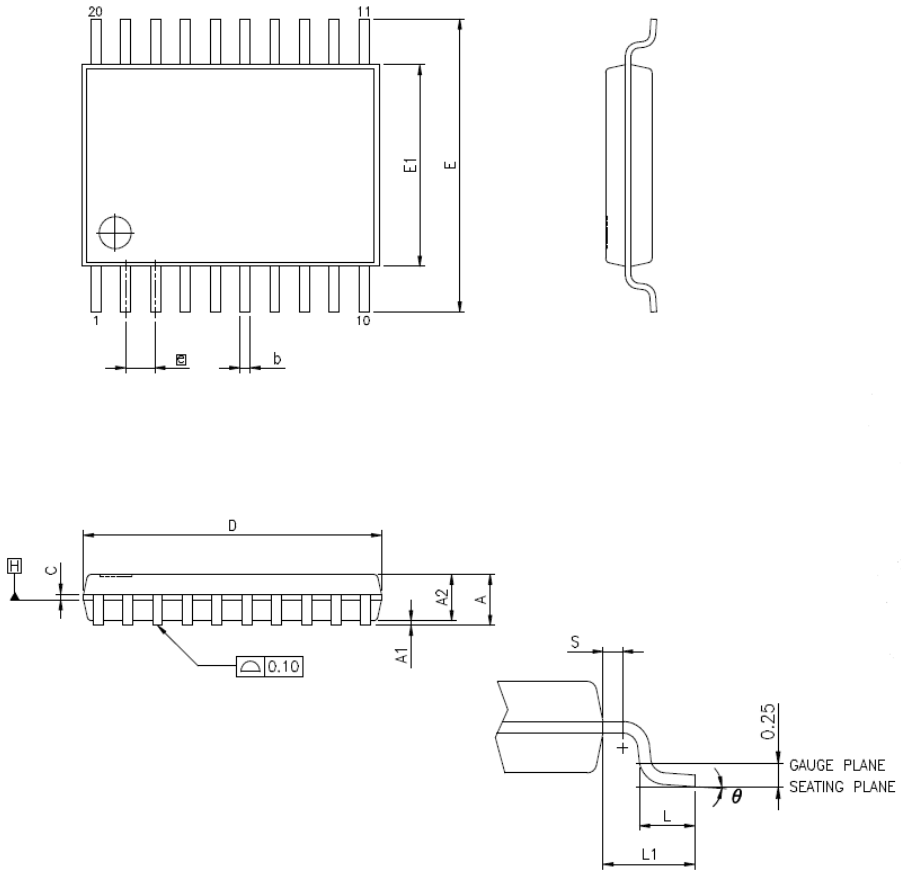




JEDEC OUTLINE	MO-220		
PKG CODE	WQFN(X520)		
SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.20 REF.		
b	0.25	0.30	0.35
D	5.00 BSC		
E	5.00 BSC		
e	0.65 BSC		
L	0.45	0.55	0.65
K	0.20	—	—

	E2			D2		
PAD SIZE	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
130X130 MIL	3.00	3.10	3.15	3.00	3.10	3.15

13.2 TSSOP 20L 4.4x6.5 MM^2



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	1.04	1.12	1.20
A1	0.05	0.10	0.15
A2	0.80	0.90	1.05
b	0.19	0.25	0.30
C	0.09	0.15	0.20
D	6.40	6.50	6.60
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.55	0.65	0.75
L1	0.80	1.00	1.20
L	0.50	0.60	0.75
S	0.20	0.30	0.40
θ	0°	4°	8°

Important Notice

Nuvoton Products are neither intended nor warranted for usage in systems or equipment, any malfunction or failure of which may cause loss of human life, bodily injury or severe property damage. Such applications are deemed, "Insecure Usage".

Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, the control or operation of dynamic, brake or safety systems designed for vehicular use, traffic signal instruments, all types of safety devices, and other applications intended to support or sustain life.

All Insecure Usage shall be made at customer's risk, and in the event that third parties lay claims to Nuvoton as a result of customer's Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.